



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,786	01/21/2004	Theodore C. White	MP0795	3539
26703	7590	09/06/2006	EXAMINER	
HARNESSE, DICKEY & PIERCE P.L.C.			SUN, SCOTT C	
5445 CORPORATE DRIVE			ART UNIT	
SUITE 400			PAPER NUMBER	
TROY, MI 48098			2182	

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 10/761,786	Applicant(s) WHITE ET AL.	
	Examiner Scott Sun	Art Unit 2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 01 May 2006.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 14-41 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 14-41 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. Applicant's request for continued examination has been received. However, Continued examination under 37 CFR 1.114 does not apply to an application unless prosecution in the application is closed. Because the RCE was accompanied by a reply to a non-final Office action, the reply will be entered and considered under 37 CFR 1.111.

### ***Response to Amendment***

2. Applicant's amendments to the claims have been noted and entered. Previous rejections are withdrawn.

### ***Response to Arguments***

3. Applicant's arguments with respect to claims 14-41 have been considered but are moot in view of the new ground(s) of rejection.

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Art Unit: 2182

5. Claims 14-16, 18, 19, ~~24~~<sup>14</sup> 26, 28, 29, 31-35, 37, 38, 40, 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aruga (US 2003/0097525) in view of Budd et al (US Patent # 7,003,702).

6. Regarding claim ~~14~~<sup>14</sup> Aruga discloses a storage controller (disk array controller 1, figure 2), comprising: a read assembly module (parity generator 9 and host and disk interface controllers), that receives a request to read the first and second data segments from a host, that extracts the first and second data segments from a plurality of data blocks, and that transfers the first and second data segments contiguously to the host (paragraph 28). Examiner notes that Aruga teaches when transferring data to the host, data segments are concatenated in the parity data generator and subsequently transferred to the host. Furthermore, the data need to be stored in the storage controller during the processing, and therefore the storage controller contains memory that stores the plurality of blocks that include first and second noncontiguous data segments.

Aruga does not teach a queue module that stores data lengths and data start addresses of the first and second data segments. However, Budd teaches a queue module (scatter-gather list) that stores data lengths (size field 902b) and data start addresses (ptr field 902a) of the first and second data segments (column 23, lines 23-37). Teachings of Aruga and Budd are from the same field of storage systems, and specifically of transferring data from disk storage to host.

Therefore, it would have been obvious at the time of invention for a person of ordinary skill in the art to implement a scatter-gather list in the system of Aruga for the

Art Unit: 2182

benefit of mapping physical location or logical location of the data. Examiner further notes that such information (address and length of data) would also be needed for the concatenation of the data segments as disclosed by Aruga.

7. Regarding claims 15, Aruga and Budd combined disclose claim 14, and Aruga further discloses wherein the plurality of data blocks include data integrity data (parity data, paragraph 27). Examiner notes that parity data is generated for storing with the raw data, which is later used to check for error detection when retrieving data from disk.

8. Regarding claim 16, Aruga and Budd combined disclose claim 15 but do not disclose explicitly using CRC as the type of integrity verification data. However, examiner notes that CRC is a widely known type of error correction/detection method at the time of invention. Given the teachings of Aruga to use integrity data, it would have been obvious for one of ordinary skill in the art at the time of invention to implement CRC as the type of integrity data because they are simple to implement in binary hardware, are easy to analyze mathematically, and are particularly good at detecting common errors.

9. Regarding claim 18, Aruga and Budd combined disclose claim 14, and Aruga further discloses wherein the read assembly module concatenates the first and second data segments (paragraph 28).

10. Regarding claim 19, Aruga and Budd combined disclose claim 14, and Aruga further discloses a second memory (cache memory 8), wherein the read assembly module transfers the first and second data segments to the second memory and the

Art Unit: 2182

second memory transfers the first and second data segments to the host (paragraph 28).

11. Claims 24-26, 28, 29, 31-35, 37, 38, 40, 41 are substantially similar to claims 14-16, 18, 19 above. They are rejected using the same arguments. Examiner notes that the storage device in teachings of Aruga and Budd are disk drives.

12. Claims 21-23, 31, 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aruga (US 2003/0097525) in view of Budd et al (US Patent # 7,003,702) and further in view of applicant's admitted prior art.

13. Regarding claim 21, Aruga, and Budd combined disclose claim 14, but does not disclose explicitly the first memory is a buffer memory. However, applicant's admitted prior art further discloses wherein the first memory is a buffer memory. Teachings of Aruga, Budd, and applicant's admitted prior art are from the same field of storage systems, and specifically of transferring data from disk storage to host.

Therefore, it would have been obvious at the time of invention to combine teachings of Aruga and Budd, and further with teachings of applicant's admitted prior art by using a buffer as memory to hold data segments for the benefit of temporarily storing data being transferred to compensate for speed differences between host and disk storage.

14. Regarding claim 22, Aruga, Budd, and applicant's admitted prior art combined disclose claim 14, and applicant's admitted prior art further discloses wherein the buffer

Art Unit: 2182

memory receives the first and second data segments from a storage device (paragraph 5, 6).

15. Regarding claim 23, Aruga, Budd, and applicant's admitted prior art combined disclose claim 14, and Aruga further discloses wherein the storage device is a hard disk drive (figure 1).

16. Claims 17, 27, 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aruga in view of Budd and applicant's admitted prior art, and further in view of Wyatt et al (PG Pub# 2003/0172325).

17. Regarding claim 17, Aruga, Budd, and applicant's admitted prior art combined disclose claim 15 but does not disclose explicitly not transferring data integrity verification data to the host. However, Wyatt teaches that data integrity verification data (parity data) is removed and not sent to the host (paragraph 10). Teachings of Wyatt, Aruga, Budd, and applicant's admitted prior art are from the same field of storage devices, and specifically of transferring data from device to host.

Therefore, it would have been obvious at the time of invention to combine teachings of Aruga, Budd, applicant's admitted prior art, and further with teachings of Wyatt by deleting integrity verification data before sending data to the host for the benefit of efficient bandwidth use.

18. Claims 27 and 36 are substantially similar to claim 17 above. They are rejected using the same arguments.

Art Unit: 2182

19. Claims 20, 30, 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aruga in view of Budd and applicant's admitted prior art, and further in view of Proch et al (PG Pub 2001/0054121).

20. Regarding claim 20, Aruga, Budd, and applicant's admitted prior art combined disclose claim 15 but does not disclose the second memory is a FIFO buffer. However, Proch teaches that FIFOs are used for data transfers from disk drive to host and vice versa (paragraphs 8-11). Teachings of Proch, Aruga, Budd, and applicant's admitted prior art are from the same field of storage devices, and specifically of transferring data from device to host.

Therefore, it would have been obvious at the time of invention to combine teachings of Aruga, Budd, applicant's admitted prior art, and further with teachings of Proch by storing the data in a FIFO buffer before sending to the host for the benefit transfer speed synchronization between host and storage device.

21. Claims 30 and 39 are substantially similar to claim 20 above. They are rejected using the same arguments.



***Conclusion***

22. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.


23. Other publications are cited to further show the state of the art with respect to data concatenation (scatter-gather) from storage devices (Parks et al) and CRC data removal (LaBerge et al). Refer to form 892, "Notice of References Cited", for a complete list of relevant prior arts cited by the examiner.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Sun whose telephone number is (571) 272-2675. The examiner can normally be reached on M-F, 10:30am-7pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim N. Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS



KIM HUYNH  
SUPERVISORY PATENT EXAMINER  
8/21/06